REMARKS/ARGUMENTS

Reconsideration of this application is respectfully requested.

Initially, the Examiner's attention is drawn to applicant's Information Disclosure Statement concurrently filed with this application on November 22, 2000. A copy of same is attached for the Examiner's convenience and return of a fully initialed copy indicating consideration of both references cited on the attached Form PTO-1449 is respectfully requested. A copy of the postcard receipt evidencing the filing of this IDS on November 22, 2000 is also attached.

The rejection of claims 1-3, 6, 9, 11 and 14 under 35 U.S.C. §102 as allegedly anticipated by Sugita '994 is respectfully traversed.

The Examiner relies upon Sugita's Figure 2B and the text at 4:17-36 – which actually describes only the writing into two separate EPROM AB via a common functional terminal. The memory maps in Figures 2A and 2B actually illustrate how a given program can be written into each separate EPROM via a common writing bus by changing each EPROM serving as a separate memory space for normal use (as shown in Figure 2A) into the same memory space when the program is written (Figure 2B).

Although the Examiner's remarks seem to be an attempt to paraphrase of the applicant's claim language, there does not appear to be any actual factual basis for such paraphrasing in the cited reference text.

Indeed, Sugita '994 at 3:42-44 describes a plurality of CPUs each having its own respective EPROM. It fails to teach plural CPUs sharing the reading of a single memory structure. Indeed, Figure 2B does not even teach the storing of data to be commonly used by a plurality of CPUs.

Applicant's claim 1 requires a first CPU to be programmed to check whether a second CPU is already accessing a non-volatile memory before the first CPU itself tries to access the non-volatile memory. The first CPU also sends to the second CPU a notification of the intended access when it discovers that the second CPU is not already involved in accessing the common shared memory space. The first CPU also stops notification to the second CPU after its completed its access to the memory (thus leaving the memory accessible to the second CPU as needed). There is nothing of this nature in the cited reference.

Applicant's independent claim 6 requires a first CPU to be programmed so as to transmit a data retrieving command and wherein both the first and second CPUs are programmed to simultaneously receive the same data from the non-volatile memory that is being retrieved in response to the data retrieving command of the first CPU – thereby

permitting both CPUs to share the same retrieved data. There is nothing to this effect in the cited reference.

Independent claim 11 is a method claim which requires the first CPU to generate a data retrieving command and to notify the second CPU of that event, to have data retrieved in response to that data retrieving command from the first CPU and then to have such data retrieved by at least the first CPU directly from the memory. Once again, there is no such teaching or suggestion anywhere in Sugita '994.

Dependent claims 2, 3, 9 and 14 add yet further patentable distinctions to the claimed invention.

The rejection of claims 4, 5, 7, 8, 10, 12, 13 and 15-30 [sic:20] under 35 U.S.C. §103 as allegedly being made "obvious" based on Sugita in view of Brauninger et al. '263 is also respectfully traversed.

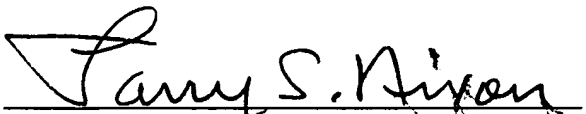
In view of the fundamental deficiencies of the primary Sugita et al. reference already noted above, it is not believed necessary at this time to further detail the deficiencies of the secondary Brauninger reference – which is also similarly deficient in its own right.

The Examiner's attention is drawn to new claims 21-23 which depend respectively from claims 1, 6 and 11 and also add further patentable distinction.

Accordingly, this entire application is now believed to be in allowable condition and a formal Notice to that effect is respectfully solicited.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: 
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